Improved Three-Dimensional GaAs Inductors

Belinda Piernas, Kenjiro Nishikawa, Kenji Kamogawa*, Tadao Nakagawa and Katsuhiko Araki

NTT Network Innovation Laboratories, 1-1 Hikarinooka,
Yokosuka-shi, Kanagawa-ken, 239-0847 Japan
* NTT DoCoMo Inc., 3-5 Hikarinooka, Yokosuka-shi, Kanagawa-ken, 239-8536 Japan

***Abstract* — This paper clarify the state-of-the-art GaAs inductors fabricated using the three-dimensional (3-D) MMIC technology. A novel 3-D inductor is proposed and evaluated experimentally. Our 4.9 nH inductance achieves a peak Q factor of 35.93 with a resonant frequency of 8.07 GHz. To the knowledge of the authors, this performance is the highest yet reported for GaAs on-chip inductors. A 0.6-4 GHz band LNA is fabricated using 0.15µm GaAs PHEMT transistors (f_{max}=120 GHz) and the 3-D inductors. The fabricated LNA offers 12.3 dB gain and a noise figure under 1.5 dB with a d.c. power consumption of 27.84 mW.**

I. INTRODUCTION

The GaAs 3-D MMIC technology has already been demonstrated to be very effective for developing compact and highly integrated microwave/millimeter-wave integrated circuits [1], [2]. However, under the C-band, the 3-D MMIC technology is somewhat limited by the lack of spiral inductors with high quality factors. Indeed, at these frequencies, spiral inductors, used either as matching networks, bias chokes, resonator elements, or circuit components, play a major role in the design of compact circuits.

The aim of the present paper is to overcome the above shortcoming and extend the capabilities of the 3-D MMIC technology to the L and S-bands. Therefore, in order to clarify the performance of 3-D inductors, we fabricated several spiral inductors with an open ground plane 10 µm under the spiral. This topology makes the proposed 3-D inductors very similar to coplanar wave-guide inductors formed on a semi-insulating substrate, and the same order of peak Q factor can be achieved. The proposed 3-D inductors are therefore suited to the realization of, up to the C-band, broadband LNAs, matching networks, and noise filters for which a moderate Q factor is adequate. For applications requiring higher Q factors, we propose a novel inductor topology that more fully utilizes the potential of the 3-D MMIC technology. This topology strongly reduces the series resistance of the inductor resulting in a high peak-Q factor.

A low noise amplifier fabricated using the 3-D inductors is also presented. The measured results confirm that the use of the 3-D MMIC technology can be extended to lower frequency applications and so can cover all microwave and millimeter-wave frequencies, from the L-band to the V-band. This is particularly interesting for designing future V-band wireless communication systems which require single-chip transceivers with IF components.

II. MODERATE-Q FACTOR 3-D INDUCTORS

A. Structure

Fig. 1 shows a typical 3-D GaAs inductor as fabricated. The spiral pattern consists in a 2 µm-thick low loss TFMS line formed on the top-level conductor layer of the 3-D MMIC process. A 1 µm-thick TFMS line located 2.5 µm under the spiral pattern is used for the inductor underpass. The open ground plane is formed on the lower-level conductor layer of the 3-D MMIC process, 10 µm under the spiral pattern.

The position of the ground plane under the spiral pattern and the low effective dielectric constant of the polyimide layer make this 3-D inductor very similar to a coplanar wave-guide GaAs inductor formed on a S.I. substrate. Therefore, the peak Q factor of these inductors is expected to be comparable to that of GaAs coplanar inductors.

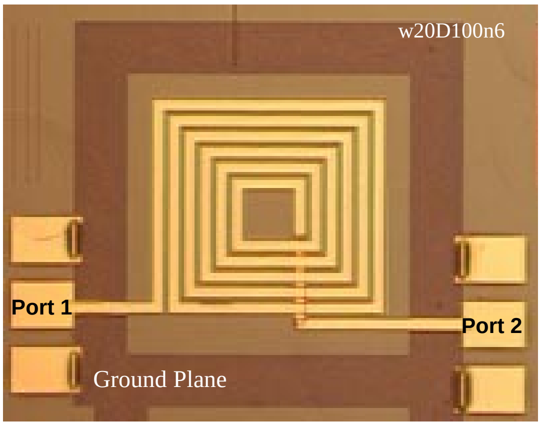

Fig. 1. Photograph of a fabricated 6 turn, 20 µm-line width, 3-D inductor with internal diameter D=100 µm.

0-7803-6540-2/01/$10.00 (C) 2001 IEEE

TABLE I

MODEL PARAMETERS OF THE MODERATE-Q FACTOR 3-D INDUCTORS

Structure #	Dimensions (µm)			Lumped-element Equivalent Circuit Parameters					F_{res} (GHz)	Peak Q
	W (µm)	D (µm)	n	L (nH)	R (Ω)	C_1 (pF)	C_2 (pF)	C_3 (pF)		
w20D20n6	20	20	6	5.275	3.802	0.084	0.0605	0.012	7.07	23.71
w20D60n6	20	60	6	6.80	4.418	0.094	0.0685	0.01	5.96	22.18
w20D100n6	20	100	6	8.81	5.449	0.105	0.0765	0.01	4.99	19.49
w10D20n4	10	20	4	1.106	2.069	0.0343	0.0171	0.000	25.82	33.39
w10D60n4	10	60	4	2.016	3.153	0.0375	0.0214	0.003	17.61	27.22
w10D100n4	10	100	4	2.936	4.156	0.0427	0.0298	0.000	14.21	24.27

B. Fabrication and Experimental Results

Several structures of the 3-D GaAs inductors with line widths, w, of 10 µm and 20 µm have been fabricated. The inductors have a constant line-to-line spacing, s, of 10 µm. The ground window surrounds the spiral pattern with a gap of 20 µm for w=10 µm and 50 µm for w=20 µm. The GaAs substrate is 600 µm thick.

The inductors have been characterized on-wafer from 0.5 to 20 GHz. The measurement of open and shorted pad reference circuits allowed the RF pads of the DUT to be de-embedded. Fig. 2 shows the two-port lumped-element model of the inductors and Table I summarizes the model values extracted from the measurements. The Q factor and the resonant frequency given in Table I were deduced from the 1-port S-parameter of the inductor when a perfect short is placed at output port 2 (see Fig. 2).

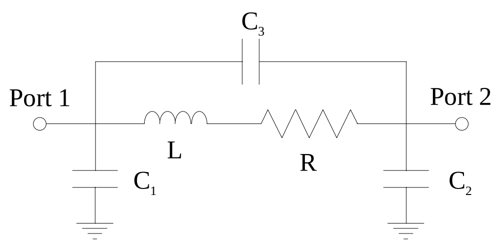

Fig. 2. Lumped-element equivalent circuit model of the 3-D inductors.

Fig. 3 shows the peak Q factor of the fabricated inductors versus the inductance. The peak Q factor of the 3-D inductors simulated with the Sonnet® software for different number of turn n is also presented. The measured results are in good agreement with the simulated results. Fig. 3 also shows that in order to achieve the highest peak Q factor, it is better to choose the 10 µm-line width structure for inductance less than 2.3 nH, and the 20 µm-line width structure for inductance greater than 2.3 nH.

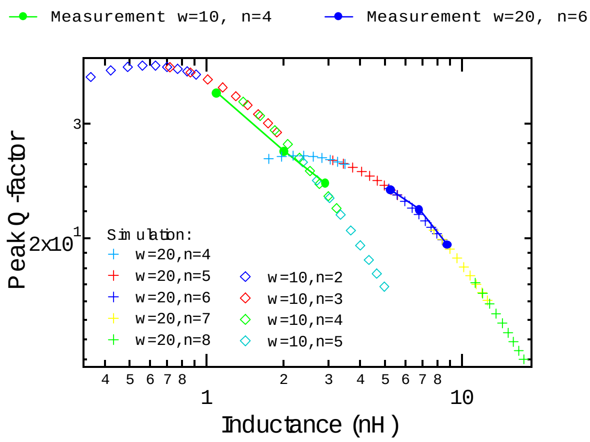

Fig. 3. Measured and simulated peak Q factor of the 3-D inductors versus the inductance.

A comparison against the state-of-the-art GaAs inductors (see Fig. 4) shows that the proposed 3-D inductors exhibit comparable performances to coplanar GaAs inductors of equivalent size. Therefore, we can conclude from this first study that the 3-D MMIC technology is adequate under the C-band, for the design of broadband low noise amplifiers and noise filters whose Q factor requirements are moderate. For applications where a high Q factor is required, we propose the novel 3-D inductor topology described below.

III. HIGH-Q FACTOR 3-D INDUCTORS

A. Structure

The originality of the proposed 3-D inductor is the combination of two superposed lines to form the spiral pattern. This configuration appreciably reduces the series resistance of the inductor which greatly increases the Q factor. This effect is slightly offset by an increase in the

TABLE II

MODEL PARAMETERS OF THE HIGH-Q FACTOR 3-D INDUCTORS

Structure #	Dimensions (µm)			Lumped-element Equivalent Circuit Parameters					F_{res} (GHz)	Peak Q
	W (µm)	D (µm)	n	L (nH)	R (Ω)	C_1 (pF)	C_2 (pF)	C_3 (pF)		
w20D20n6_56	20	20	6	4.9	2.66	0.0794	0.1356	0.0	8.07	35.93
w20D60n6_56	20	60	6	6.46	3.192	0.0944	0.1506	0.0	6.44	31.53
w20D100n6_56	20	100	6	8.08	3.832	0.1094	0.1656	0.0	5.35	27.28

inductor's parasitic capacitance due to the coupling between the lines, but the increase in the peak Q factor remains significant. Fig. 5 shows the cross section of the proposed high-Q factor inductor fabricated using the 3-D MMIC process. The inductor is formed by two identical spiral patterns that are stacked on the top-level and the second-level conductor layers of the 3-D MMIC process.

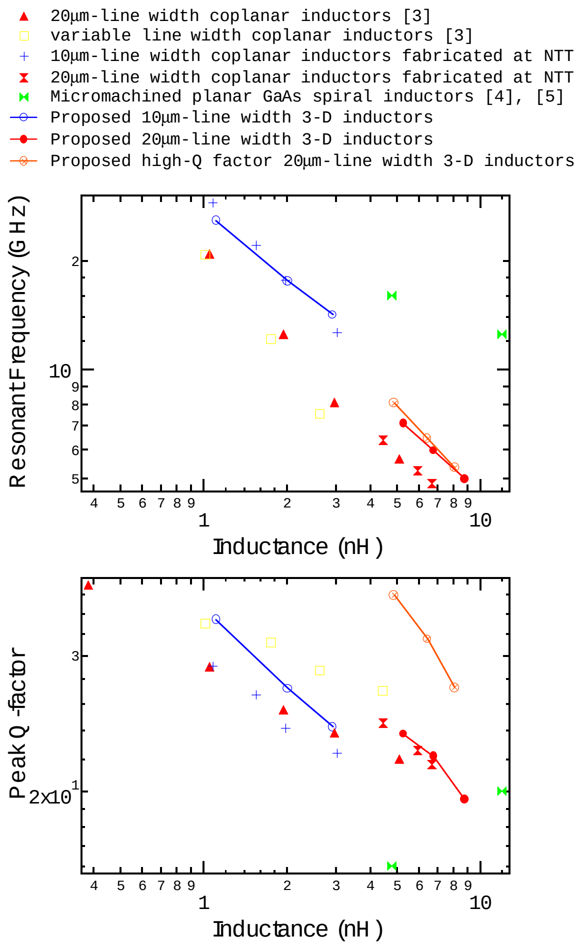

Fig. 4. State-of-the-art GaAs inductors compared to the proposed 3-D inductors.

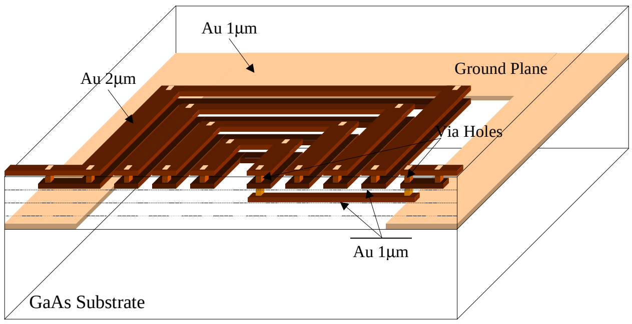

Fig. 5. Cross section of the proposed high-Q factor inductor fabricated using the 3-D MMIC technology.

The top-level spiral pattern is 2 µm thick and the other is 1 µm thick. These two patterns are interconnected at regular intervals by via-holes through the first dielectric layer. The underpass of the inductor is a 1 µm-thick TFMS line formed on the third conductor layer (2.5 µm under the second spiral pattern). The open ground plane is formed on the lower-level conductor layer of the 3-D MMIC process, 10 µm under the first spiral pattern.

B. Fabrication and Experimental Results

Fig. 6 shows an example of the new 3-D inductors. Three spiral inductors were fabricated with internal diameters, D, of 20 µm, 60 µm, and 100 µm. All uses 6 turns of superposed 20 µm-width TFMS lines. The line-to-line spacing, s, is 10 µm and the gap, G, to the ground window is 50 µm. The GaAs substrate thickness is 600 µm.

The inductors were characterized on-wafer from 0.5 to 20 GHz. The two-port lumped-element model of the inductors is shown in Fig. 2 and Table II summarizes the model parameters extracted from the S-parameter measurements. For a 4.9 nH inductor, a very high peak-Q factor of 35.93 is achieved at 4.66 GHz. The resonant frequency of this inductor is 8.07 GHz. Compared to the state-of-the-art GaAs inductors shown in Fig. 4, the novel 3-D inductors exhibit very high peak-Q factors, the highest yet reported.

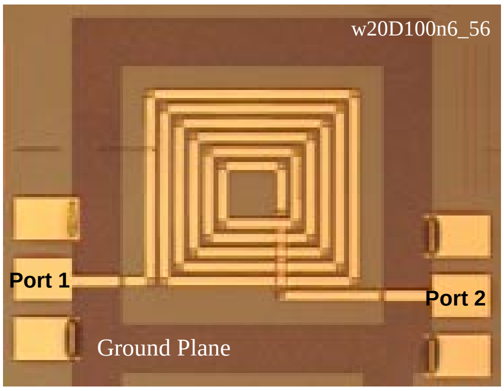

Fig. 6. Photograph of a high-Q factor 3-D inductor.

IV. 0.6-4 GHz Band Low Noise Amplifier

We designed a 0.6-4 GHz band low noise amplifier to confirm the potential of the 3-D inductors presented in section II. Fig. 7 (a) shows a photograph of the LNA fabricated using the 3-D MMIC technology. The chip size is 1.52×1.17 mm^2. The transistors are 0.15 µm long, 100 µm wide PHEMTs whose minimum noise figure is 0.36 dB at 12 GHz, f_T is 70 GHz, and f_{max} is 120 GHz.

The performances of the LNA are shown in Fig. 7 (b). It exhibits broadband operation, from 0.6 GHz to 4 GHz with a gain above 12.3 dB and a noise figure under 1.5 dB. The return losses at the input and the output ports are less than –3.6 dB and –5 dB, respectively. The d.c. power consumption of the amplifier is 27.84 mW.

These performances show that the proposed broadband low noise amplifier, based on the moderate Q-factor inductors, is competitive with low noise amplifiers fabricated using a planar technology [6].

V. Conclusion

We have clarified the performances of GaAs 3-D inductors and demonstrated that the 3-D MMIC technology is not limited to high frequencies by the lack of efficient inductors. This is confirmed by the fabrication of a 0.6-4 GHz LNA using the 3-D inductors.

Since some applications will require extremely high peak-Q factors, we proposed a new 3-D inductor topology that fully uses the capability of the 3-D process. A 4.9 nH inductor is fabricated and found to offer a peak-Q factor of 35.93. To the best of our knowledge, this value is the highest yet reported for GaAs inductors.

Moreover, considering these promising results, we have simulated and fabricated a 3-level conductor layers inductor using the 3-D MMIC technology. The experimental results will be detail in conference.

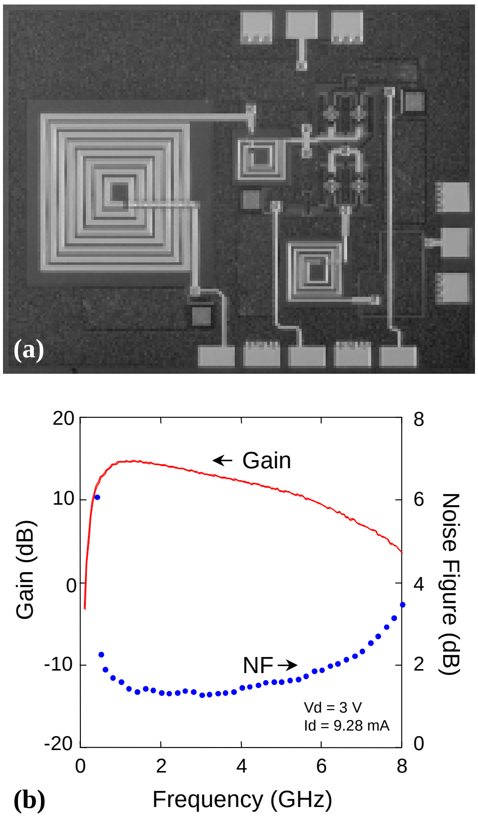

Fig. 7. (a) Photograph and (b) measured performances of the 0.6-4 GHz band LNA designed using the 3-D inductors.

References

[1] I. Toyoda, T. Tokumitsu, and M. Masayoshi, "Highly integrated three-dimensional MMIC single-chip receiver and transmitter," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-44, no. 12, pp. 2340-2346, Dec. 1996.

[2] K. Nishikawa, K. Kamogawa, K. Inoue, K. Onodera, T. Tokumitsu, M. Tanaka, I. Toyoda, and M. Hirano, "Miniaturized millimeter-wave masterslice 3-D MMIC amplifier and mixer," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-47, no. 9, pp. 1856-1862, Sep. 1999.

[3] I. J. Bahl, "Improved quality factor spiral inductor on GaAs substrates," *IEEE Microwave and Guided Wave Lett.*, vol. 9, no. 10, pp. 398-400, Oct. 1999.

[4] R. P. Ribas, J. Lescot, J. L. Leclercq, N. Bernnouri, J. M. Karam, and B. Courtois, "Micromachined planar spiral inductor in standard GaAs HEMT MMIC technology," *IEEE Electron Device Lett.*, vol. 19, no. 8, pp. 285-287, Aug. 1998.

[5] R. P. Ribas, J. Lescot, J. L. Leclercq, J. M. Karam, and F. Ndagijimana, "Monolithic micromachined planar spiral transformer," *IEEE GaAs IC Symp. Dig.*, Techn. Dig. 1998, pp. 255-258, Nov. 1998.

[6] B. K. Ko, and K. Lee, "A comparative study on the various monolithic low noise amplifier circuit topologies for RF and microwave applications," *IEEE Journal of Solid-State circuits*, vol. 31, no. 8, pp. 1220-1225, Aug. 1996.